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#### ABSTRACT

0026 An ILD dielectric layer stack and method for forming the same, the method includes a semiconductor substrate including CMOS transistors with gate electrode portions; depositing a first layer including phosphorous doped SiO<sub>2</sub> over the semiconductor substrate to a thickness sufficient to cover the gate electrode portions including intervening gaps; depositing a second layer of undoped SiO<sub>2</sub> over and contacting the first layer to a thickness sufficient to leave a second layer thickness portion overlying the first layer following a subsequent oxide chemical mechanical polish (CMP) planarization process; carrying out the oxide CMP process to planarize the second layer and leave the second layer thickness portion; and forming metal filled local interconnects extending through a thickness portion of the first and second layers.